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jc682 U.S. PTO 02/24/00

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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1343
First Inventor or Application Identifier	Robert Kerr
Title	See 1 in Addendum
Express Mail Label No.	EL465677729US

jc525 U.S. PTO 09/511978 02/24/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)

2. [X] Specification [*Total Pages* 24]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 3]

4. Oath or Declaration [*Total Pages* 8]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d))
   (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [X] Other: $690.00 check
Change of Correspondence Address

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09/146,115
Prior application information: *Examiner* R. Hullinger *Group / Art Unit:* 2825

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 021567 *(Insert Customer No. or Attach bar code label here)* *or* [ ] *Correspondence address below*

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Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Bernard Berman	*Registration No. (Attorney/Agent)*	37,279
Signature	Bernard Berman	*Date*	Feb 24, 2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

EL465677729

Addendum

1. Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, and Integrated Circuits

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/146,115
Priority Filing Date ..... September 2, 1998
Inventor ..... Robert Kerr et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2825
Priority Examiner ..... R. Hullinger
Attorney's Docket No. MI22-1343
Title: Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, and Integrated Circuits

PRELIMINARY AMENDMENT

To: Box PATENT APPLICATIONS
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Bernard Berman (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

Please enter the following amendments prior to examining the above-identified application.

AMENDMENTS

In the Specification:

At p. 1 before the "Technical Field" section, please insert the following:

--**RELATED PATENT DATA**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/146,115, filed September 2, 1998, entitled "Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, and Integrated Circuits," naming Robert Kerr, Brian Shirley, Luan C. Tran and Tyler A. Lowrey as inventors, and which is now U.S. Patent No. _____, the disclosure of which is incorporated by reference.--

In the Claims:

Cancel claims 9-49 without prejudice.

REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 09/146,115. Claims 9-49 have been canceled without prejudice. Claims 1-8 and 50 remain in the application for consideration. Applicant requests examination of such pending claims.

Respectfully submitted,

Dated: Feb 24, 2000

By: Bernard Berman

Bernard Berman
Reg. No. 37,279

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, And Integrated Circuits

* * * * *

INVENTORS

Robert Kerr
Brian Shirley
Luan C. Tran
Tyler A. Lowrey

ATTORNEY'S DOCKET NO. MI22-813

METHODS OF FORMING CONTACTS, METHODS OF CONTACTING LINES, METHODS OF OPERATING INTEGRATED CIRCUITRY, AND INTEGRATED CIRCUITS

TECHNICAL FIELD

This invention relates to methods of forming contacts, to methods of contacting lines, and to methods of operating integrated circuitry. The invention also relates to integrated circuits.

BACKGROUND OF THE INVENTION

Conductive lines which are utilized in integrated circuitry are often formed with widened areas called contact or landing pads. The purpose of these pads is to provide an extra degree of protection should a misalignment occur between a contact opening which is formed over the line. While advantages are gained in reducing the chances of a misalignment-induced failure, valuable wafer real estate is consumed by the widened pads.

Referring to Fig. 1, a portion of an exemplary prior art layout is shown generally at 10 and includes conductive lines 12, 14 and 16 having widened contact pads 18, 20 and 22, respectively. To conserve wafer real estate, it is usually desirable to provide conductive lines 12, 14, 16 to have a minimum pitch which is defined in large part by the minimum photolithographic feature size used to fabricate the circuitry. Minimizing the pitch of the lines ensures that the space between the lines, represented at S, is as small as possible. Yet, to

ensure that subsequently formed contacts to the conductive lines do not short to the substrate, the above-described widened contact pads are used. A design trade-off, however, is that in order to maintain a desired pitch between the conductive lines, and to avoid forming the contact pads too close together, the contact pads must necessarily be moved outwardly of one another. For example, in Fig. 1, contact pad 18 is moved outward in the direction of arrow A. Other contact pads can be spaced even further out depending on the dimensions of the contact pads. This results in consumption of valuable wafer real estate.

SUMMARY OF THE INVENTION

Methods of forming contacts, methods of contacting lines, methods of operating integrated circuitry, and related integrated circuitry constructions are described. In one embodiment, a plurality of conductive lines are formed over a substrate and diffusion regions are formed within the substrate elevationally below the lines. The individual diffusion regions are disposed proximate individual conductive line portions and collectively define therewith individual contact pads with which electrical connection is desired. Insulative material is formed over the conductive line portions and diffusion regions, with contact openings being formed therethrough to expose portions of the individual contact pads. Conductive contacts are formed within the contact openings and in electrical connection with the individual contact pads. In a preferred

embodiment, the substrate and diffusion regions provide a pn junction which is configured for biasing into a reverse-biased diode configuration. In operation, the pn junction is sufficiently biased to preclude electrical shorting between the conductive line and the substrate for selected magnitudes of electrical current provided through the conductive line and the conductive material forming the conductive contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings:

Fig. 1 is a top plan view of a portion of a prior art circuit layout.

Fig. 2 is a diagrammatic side sectional view of a semiconductor wafer fragment in accordance with one embodiment of the invention.

Fig. 3 is a diagrammatic side sectional view of the semiconductor wafer fragment in accordance with another embodiment of the invention.

Fig. 4 is a top plan view of a circuit layout in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Figs. 2-4, separate embodiments of the present invention are shown and include a semiconductor wafer fragment generally at 24 (Fig. 2), 24a (Fig. 3) including a semiconductive substrate 26. Like numerals are utilized between the figures, with differences being indicated with the suffix "a" or "b", or with different numerals. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 26 comprises a first-type dopant which can be either p-type or n-type.

A plurality of conductive lines 28 are formed over substrate 26 and include a gate oxide layer 29, polysilicon layer 30, a silicide layer 32, an insulative cap 34, and sidewall spacers 36. Other conductive line constructions are possible. Diffusion regions 38 (Fig. 2), 38a (Fig. 3), and 38b (Fig. 4) are formed within substrate 26 and elevationally lower than conductive lines 28. In one embodiment,

dynamic random access memory (DRAM) circuitry is formed over and supported by substrate 26, with conductive lines 28 comprising individual word lines. DRAM circuitry typically includes storage cells which are disposed within a memory array, and a peripheral area proximate the memory array. The storage cells include a storage capacitor which is operably coupled with a word line through a diffusion region. Storage capacitors typically include a storage node layer, a dielectric layer, and a cell plate layer. The word lines extend through the memory array and the peripheral area proximate the memory array. Diffusion regions 38 can be formed in the peripheral area of the substrate outside of the memory array.

In one embodiment (Fig. 2), diffusion regions 38 can be formed prior to formation of conductive lines 28. Such permits the conductive lines to be formed over the diffusion regions so that the diffusion regions extend directly under conductive portions of the conductive lines. In another, more-preferred embodiment (Fig. 3), two individual diffusion regions 38a are formed after formation of conductive lines 28, and on each side thereof. A pair of isolation oxide regions 39 can be provided as shown. Individual diffusion regions 38, 38a-b are disposed operably proximate respective individual conductive line portions 40 and define areas which are comprised of a second-type dopant which is different from the first-type dopant comprising the substrate. Where substrate 26 comprises p-type dopant, diffusion regions 38, 38a-b comprise n-type dopant. Conversely, where substrate 26 comprises n-

type dopant, diffusion regions 38, 38a-b comprise p-type dopant. The diffusion regions and conductive line portions 40 collectively effectively define individual contact pads 42 with which electrical and physical connection is desired. The diffusion regions and substrate provide a pn junction which can be configured into a reverse-biased diode configuration during operation, as will become apparent below.

A layer of insulative material 44 is formed over substrate 26 including line portions 40 and diffusion regions 38, 38a-b. An exemplary material is borophosphosilicate glass. Contact openings 46 are formed through layer 44 and expose portions of individual contact pads 42. Contact openings 46 can overlap with individual conductive lines and their associated diffusion regions as shown. Conductive contacts 48 are formed or deposited within contact openings 46 and in electrical connection with the individual contact pads 42. In a preferred embodiment, conductive contacts 48 comprise metal such as tungsten, including metal alloys. In the illustrated example, conductive contacts 48 provide conductive material which is received over the conductive lines and interconnects the line with its associated diffusion region. Accordingly, material of contacts 48 electrically contacts both conductive lines 28 and their respective diffusion regions 38, 38a-b.

Referring to Fig. 4, individual conductive lines 28 have second conductive line portions 50 which are joined with respective first conductive line portions 40 and in electrical communication therewith. Individual conductive lines 28 have pitches P relative to respective next

adjacent lines. At least one, and preferably a plurality of the conductive lines have a pitch P between its first conductive line portion 40 and a next adjacent line which is substantially the same as a pitch between its second conductive line portion 50 and the next adjacent line. In the illustrated example, individual conductive lines 28 each have a lateral width dimension W away from its conductive line portion 40 which is substantially equivalent to the lateral width dimension of its conductive line portion 40. Preferably, the conductive lines have substantially equivalent lateral width dimensions.

Alternately considered, each conductive line has an average lateral width dimension W. Conductive line portions 40 have lateral width dimensions which are substantially equivalent to the average lateral width dimension of its associated conductive line. Such provides the conductive lines to have a generally uniform lateral width dimension along their respective entireties.

One advantage provided by the invention is that conductive lines 28 can be formed to have pitches which are more defined by minimum photolithographic feature sizes, without the lines having widened contact pads comprising material of the conductive lines. Thus, contact openings 46 can be formed over every other line (Fig. 4) along a generally straight line 52. There is no spacing-induced need to stagger the contact openings because the widened contact or landing pads can be eliminated.

Integrated circuitry formed in accordance with the inventive methods can provide a reverse-biased pn junction elevationally lower than one or more conductive lines, e.g. lines 30, 32, and 50. Electrical current may be provided through conductive lines 30, 32, and 50 and conductive material forming conductive contacts 48, with a reverse-biased pn junction between regions 38, 38a and substrate 26 being sufficiently reverse biased to preclude electrical shorting between conductive lines 30, 32 and 50, and substrate 26. Conventionally, in a DRAM, substrate 26 is biased to a negative voltage level V_{bb} on the order of 1 volt, and it is anticipated that voltage on contact via 48 is maintained in reverse bias, e.g. 0 volts. This allows for a reduction in wafer real estate which was formerly required to accommodate the widened contact pads (Fig. 1).

As an example, where substrate 26 comprises p-type material, the substrate can be provided at a voltage potential of -1 volt, and conductive contact 48 can be grounded to provide the desired reversed bias. Where substrate 26 comprises n-type material, the substrate can be biased at a voltage potential of around 4 volts, with conductive contact 48 being biased at around 2 volts to provide the desired reversed bias. Other advantages of the present invention include a reduction in circuit layout area as well as an increased number of contacts being provided in the same substrate wafer area.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical

features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. An integrated circuit comprising a conductive line received over a semiconductive substrate and a diffusion region within the substrate proximate the line, the diffusion region and substrate forming a junction which is effectively reverse biased to preclude shorting between the conductive line and the substrate through any conductive material extending therebetween for selected magnitudes of current provided through the conductive line.

2. The integrated circuit of claim 1, wherein the conductive material comprises metal.

3. The integrated circuit of claim 1, wherein a portion of the diffusion region is disposed directly under conductive portions of the conductive line.

4. The integrated circuit of claim 1, wherein the diffusion region comprises two individual diffusion regions disposed respectively on each side of the conductive line.

5. An integrated circuit comprising a conductive line received over a semiconductive substrate and a diffusion region within the substrate proximate the line, conductive material being received over the line and interconnecting it with the diffusion region, the diffusion region being effectively reverse biased to preclude shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

6. The integrated circuit of claim 5, wherein the conductive material comprises metal.

7. The integrated circuit of claim 5, wherein a portion of the diffusion region is disposed under conductive portions of the conductive line.

8. The integrated circuit of claim 5, wherein the diffusion region comprises two individual diffusion regions disposed respectively on each side of the conductive line.

9. A method of contacting a line comprising:

providing a substrate comprising a first-type dopant;

forming a conductive line over the substrate, the line comprising a portion with which electrical connection is to be made;

forming a diffusion region within the substrate proximate the conductive line portion and comprising a second-type dopant which is different from the first-type dopant, the conductive line portion and diffusion region forming a contact pad for the conductive line; and

forming conductive material in electrical contact with the contact pad.

10. The semiconductor conductive line-contacting method of claim 9, wherein the forming of the conductive material comprises forming metal material in electrical contact with the contact pad.

11. The semiconductor conductive line-contacting method of claim 9, wherein the first-type dopant comprises n-type dopant.

12. The semiconductor conductive line-contacting method of claim 9, wherein the first-type dopant comprises p-type dopant.

13. The semiconductor conductive line-contacting method of claim 9, wherein the forming of the conductive line comprises forming the conductive line to have an average lateral width dimension, and wherein the conductive line portion has a lateral width dimension which is substantially equivalent to the average lateral width dimension.

14. The semiconductor conductive line-contacting method of claim 9, wherein the forming of the conductive line comprises forming the conductive line to have a generally uniform lateral width dimension along its entirety.

15. The semiconductor conductive line-contacting method of claim 9, wherein the forming of the diffusion region defines a pn junction within the substrate, and further comprising reverse biasing the pn junction.

16. The semiconductor conductive line-contacting method of claim 9, wherein the forming of the diffusion region defines a pn junction within the substrate, and further comprising reverse biasing the pn junction after the forming of the conductive material.

17. A method of forming a contact comprising:

forming a plurality of conductive lines over a substrate;

forming diffusion regions within the substrate and elevationally below the conductive lines, individual diffusion regions being disposed proximate respective individual conductive line portions, individual conductive line portions and individual associated diffusion regions collectively effectively defining individual contact pads with which electrical connection is desired for the individual conductive lines;

forming insulative material over the conductive line portions and diffusion regions;

forming contact openings through the insulative material over and exposing portions of the individual contact pads; and

forming conductive contacts within the contact openings and in electrical connection with individual contact pads.

18. The method of forming a contact of claim 17, wherein the forming of the conductive contacts comprises depositing metal within the contact openings.

19. The method of forming a contact of claim 17, wherein the forming of the plurality of conductive lines comprises forming one of the conductive lines to have a lateral width dimension away from its conductive line portion which is substantially equivalent to the lateral width dimension of its conductive line portion.

20. The method of forming a contact of claim 17, wherein the forming of the plurality of conductive lines comprises forming individual conductive lines to have lateral width dimensions away from their respective conductive line portions which are substantially equivalent to the lateral width dimensions of their conductive line portions.

21. The method of forming a contact of claim 20, wherein the forming of the plurality of conductive lines comprises forming said conductive lines to have substantially equivalent lateral width dimensions.

22. The method of forming a contact of claim 17, wherein the substrate comprises one type dopant, and the forming of the diffusion regions comprises forming said diffusion regions with a different type dopant.

23. The method of forming a contact of claim 22, wherein the one type dopant comprises n-type dopant.

24. The method of forming a contact of claim 22, wherein the one type dopant comprises p-type dopant.

25. The method of forming a contact of claim 17, wherein the forming of the diffusion regions comprises forming said diffusion regions after forming the plurality of conductive lines.

26. The method of forming a contact of claim 17, wherein the forming of the diffusion regions comprises forming pn junctions within the substrate, and further comprising reverse-biasing the pn junctions.

27. A method of contacting a line comprising:

providing a substrate having a diffusion region formed therein, the substrate and diffusion region being configured for biasing into a reverse-biased diode configuration;

forming a conductive line over the substrate, the conductive line and diffusion region being formed operably proximate one another and collectively defining an effective contact pad with which electrical connection is desired;

forming an insulative material over the contact pad;

forming a contact opening through the insulative material and exposing at least a portion the contact pad; and

forming conductive material within the contact opening and in electrical connection with the contact pad.

28. The semiconductor conductive line-contacting method of claim 27, wherein the substrate and the diffusion region provide a pn junction.

29. The semiconductor conductive line-contacting method of claim 28, wherein the substrate comprises n-type dopant.

30. The semiconductor conductive line-contacting method of claim 28, wherein the substrate comprises p-type dopant.

31. The semiconductor conductive line-contacting method of claim 27, wherein the forming of the conductive material comprises forming said material to electrically contact both the conductive line and the diffusion region.

32. The semiconductor conductive line-contacting method of claim 27, wherein the forming of the contact opening comprises forming said opening to overlap with the conductive line and the diffusion region.

33. A method of contacting a line comprising:

providing a substrate comprising a first-type dopant;

forming a conductive line over the substrate comprising a conductive line portion with which electrical connection is to be made;

forming an area within the substrate proximate the conductive line portion and comprising a second-type dopant which is different from the first-type dopant, the conductive line portion and area forming a contact pad for the conductive line, the area and substrate defining a pn junction;

forming conductive material in electrical contact with the contact pad; and

reverse-biasing the pn junction.

34. The semiconductor conductive line-contacting method of claim 33, wherein said area extends under conductive portions of the conductive line.

35. The semiconductor conductive line-contacting method of claim 33, wherein the first-type dopant comprises p-type dopant.

36. The semiconductor conductive line-contacting method of claim 33, wherein the first-type dopant comprises n-type dopant.

37. The semiconductor conductive line-contacting method of claim 33, wherein the conductive line portion of the contact pad has a lateral width dimension which is substantially the same as a lateral width dimension of the conductive line away from the contact pad.

38. A method of forming contacts comprising:

forming a plurality of conductive lines over a substrate, individual conductive lines having first conductive line portions with which electrical and physical connection is desired and second conductive line portions which are joined with the first conductive line portions and in electrical communication therewith, individual conductive lines having pitches relative to respective next adjacent lines, at least one of the conductive lines having a pitch between its first conductive line portion and a next adjacent line which is substantially the same as a pitch between its second conductive line portion and the next adjacent line;

forming individual diffusion regions proximate the first conductive line portions of the conductive lines, the first conductive line portions and individual diffusion regions collectively effectively defining individual contact pads for the individual conductive lines, the diffusion regions and substrate providing individual respective pn junctions elevationally below the conductive lines;

forming insulative material over the conductive lines and diffusion regions;

forming contact openings through the insulative material over and exposing portions of individual contact pads;

forming conductive contacts within the contact openings and in electrical connection with individual contact pads; and

reverse-biasing the pn junctions.

39. The method of claim 38, wherein the first and second conductive line portions of said at least one conductive line have lateral width dimensions which are substantially the same.

40. The method of claim 38, wherein the first and second conductive line portions of said next adjacent line have lateral width dimensions which are substantially the same.

41. The method of claim 38, wherein:

the first and second conductive line portions of said at least one conductive line have lateral width dimensions which are substantially the same; and

the first and second conductive line portions of said next adjacent line have lateral width dimensions which are substantially the same.

42. The method of claim 38, wherein the forming of the contact openings comprises forming contact openings over every other line which are disposed along a generally straight line.

43. The method of claim 38, wherein the forming of the diffusion regions comprises forming diffusion regions on either side of the first conductive line portions of at least some of the conductive lines.

44. A method of operating integrated circuitry comprising:

providing a reverse-biased pn junction elevationally lower than a conductive line which is formed over a substrate, said junction being provided within the substrate and proximate a portion of the conductive line, the reverse-biased pn junction and the conductive line portion providing a contact pad for conductive material which is provided over and in electrical contact with the contact pad through insulative material which is provided over the conductive line portion and at least some of the pn junction; and

providing electrical current through the conductive line and conductive material, the reverse-biased pn junction being sufficiently biased to preclude electrical shorting between the conductive line and the substrate for selected magnitudes of electrical current.

45. The method of claim 44, wherein the reverse-biased pn junction comprises a diffusion region which extends under an entirety of the conductive line portion.

46. The method of claim 44, wherein the reverse-biased pn junction comprises a pair diffusion regions which extend on either side of the conductive line portion.

47. The method of claim 44, wherein the substrate comprises p-type dopant and the pn junction is defined in part by a n-type diffusion region.

48. The method of claim 44, wherein the substrate comprises n-type dopant and the pn junction is defined in part by a p-type diffusion region.

49. A method of operating integrated circuitry comprising:

providing a substrate comprising a first-type dopant;

providing a conductive line over the substrate comprising a conductive line portion;

providing a diffusion region within the substrate proximate the conductive line portion and comprising a second-type dopant which is different from the first-type dopant, the conductive line portion and diffusion region forming a contact pad for the conductive line;

providing conductive material in electrical contact with the contact pad; and

providing a voltage potential across the substrate and diffusion region sufficient to provide a reverse-biased diode construction configured to preclude shorting between the conductive line and the substrate for selected magnitudes of current provided through the conductive line.

ABSTRACT OF THE DISCLOSURE

Methods of forming contacts, methods of contacting lines, methods of operating integrated circuitry, and related integrated circuitry constructions are described. In one embodiment, a plurality of conductive lines are formed over a substrate and diffusion regions are formed within the substrate elevationally below the lines. The individual diffusion regions are disposed proximate individual conductive line portions and collectively define therewith individual contact pads with which electrical connection is desired. Insulative material is formed over the conductive line portions and diffusion regions, with contact openings being formed therethrough to expose portions of the individual contact pads. Conductive contacts are formed within the contact openings and in electrical connection with the individual contact pads. In a preferred embodiment, the substrate and diffusion regions provide a pn junction which is configured for biasing into a reverse-biased diode configuration. In operation, the pn junction is sufficiently biased to preclude electrical shorting between the conductive line and the substrate for selected magnitudes of electrical current provided through the conductive line and the conductive material forming the conductive contacts.

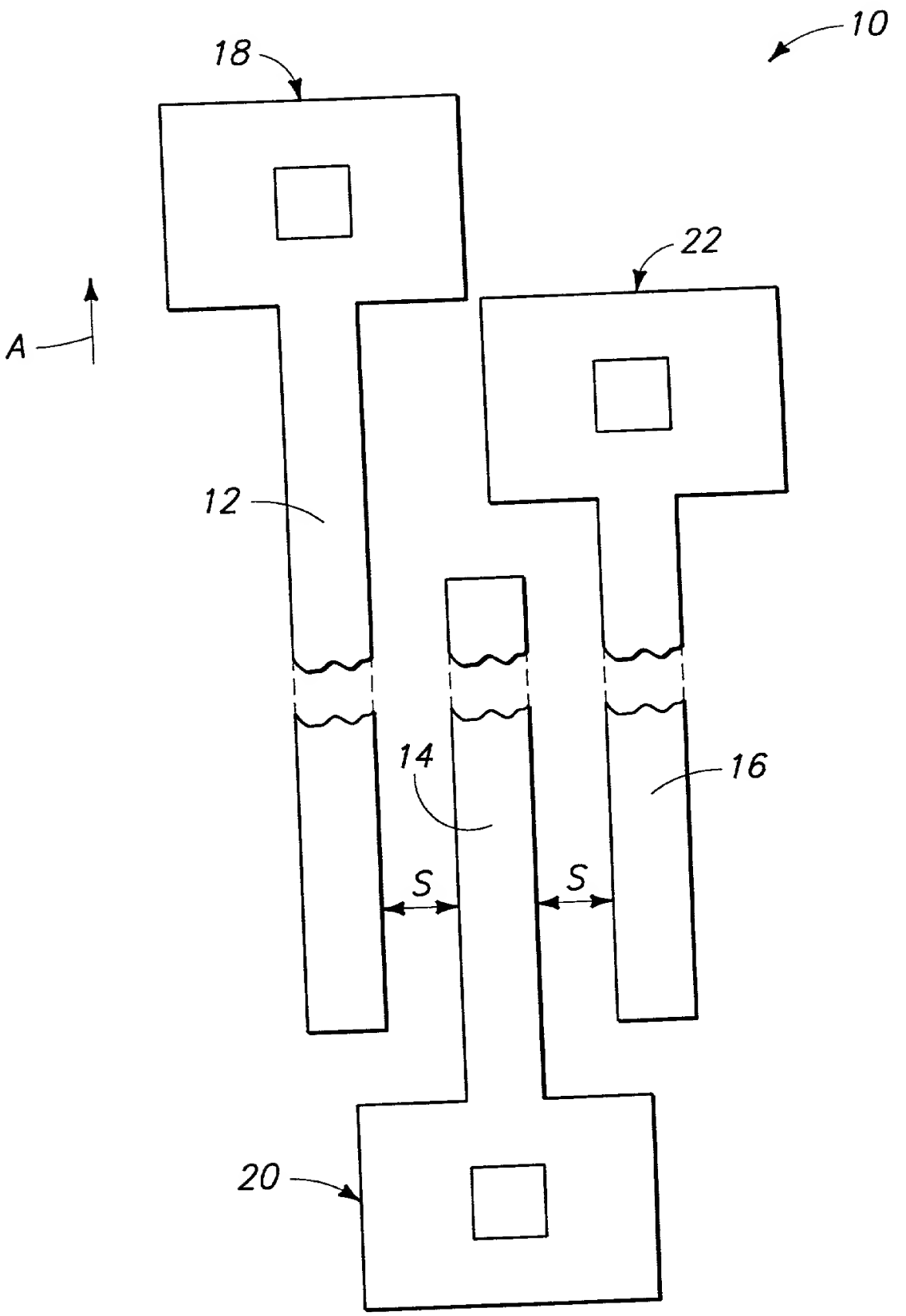

FIG 1
PRIOR ART

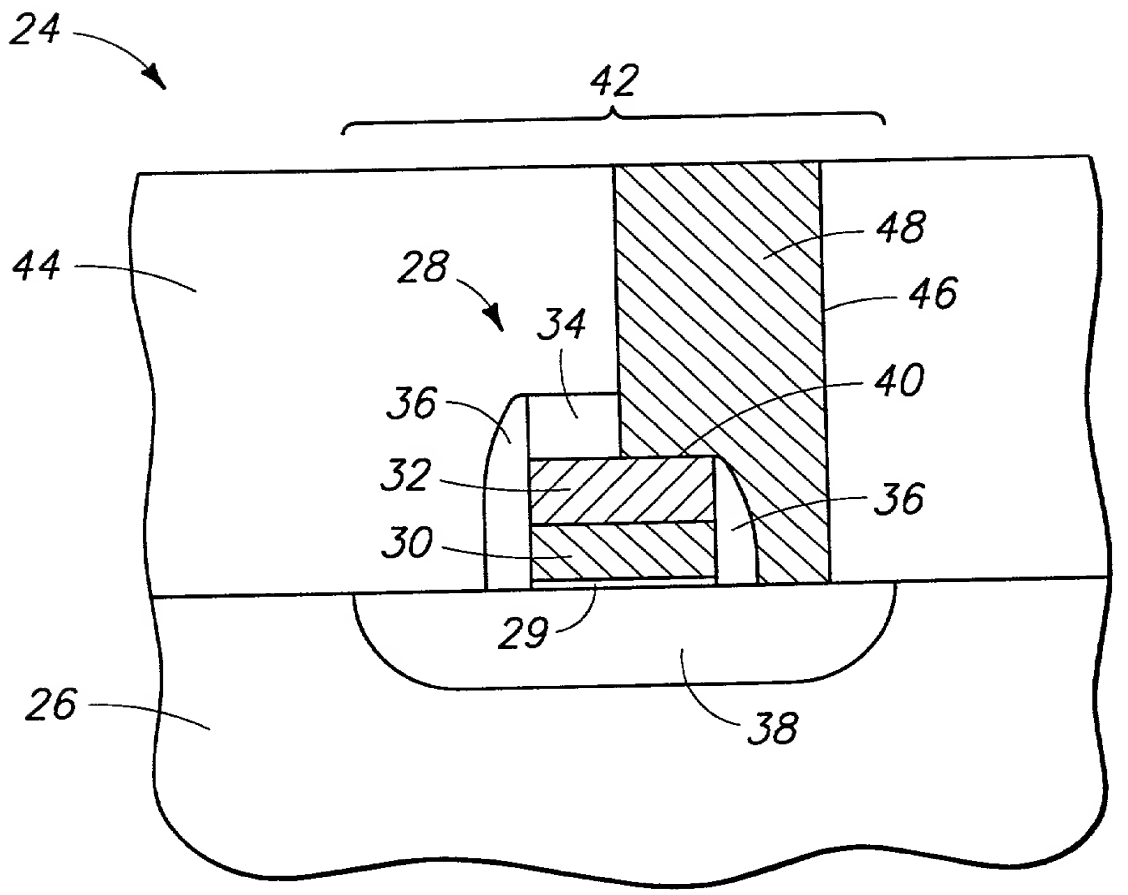
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Fig 2

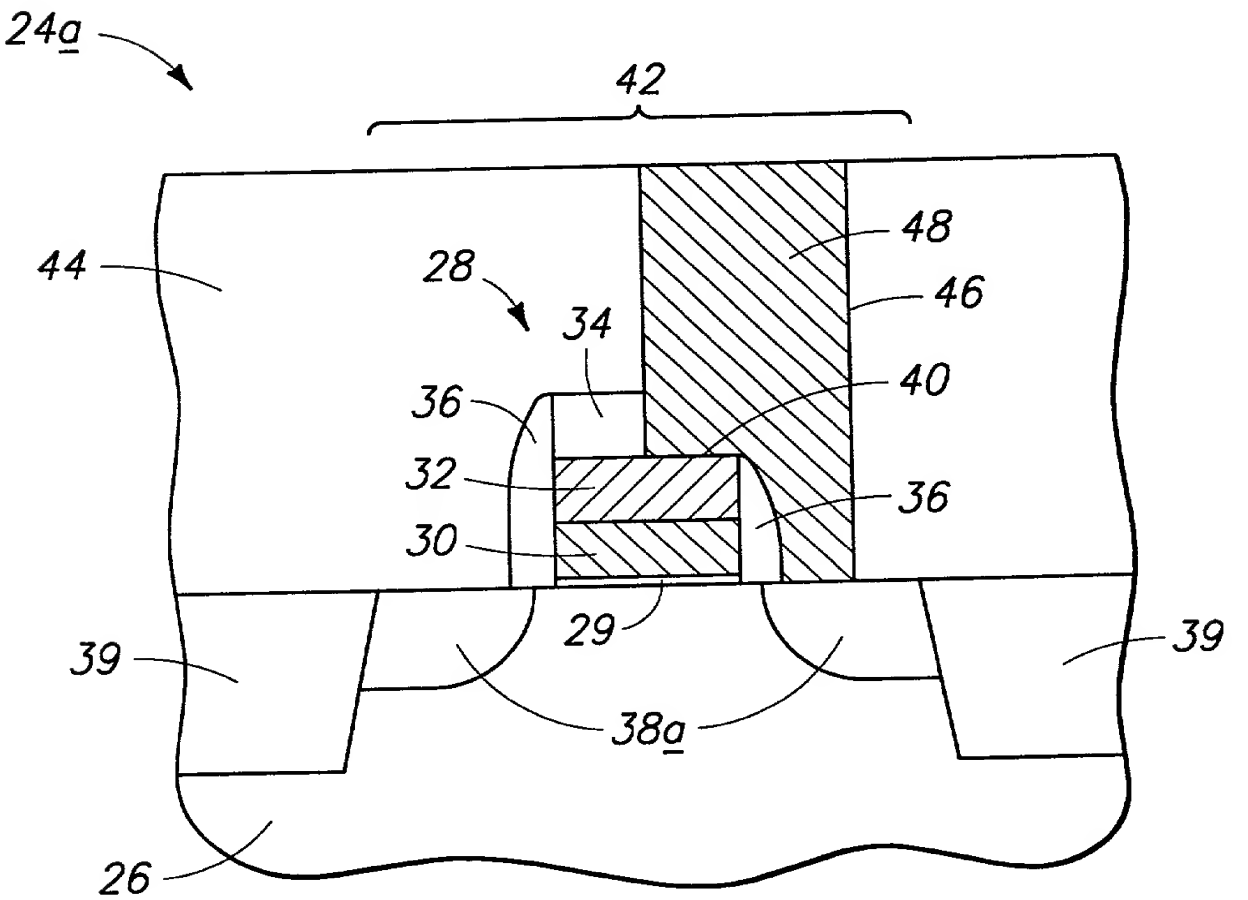
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Fig 3

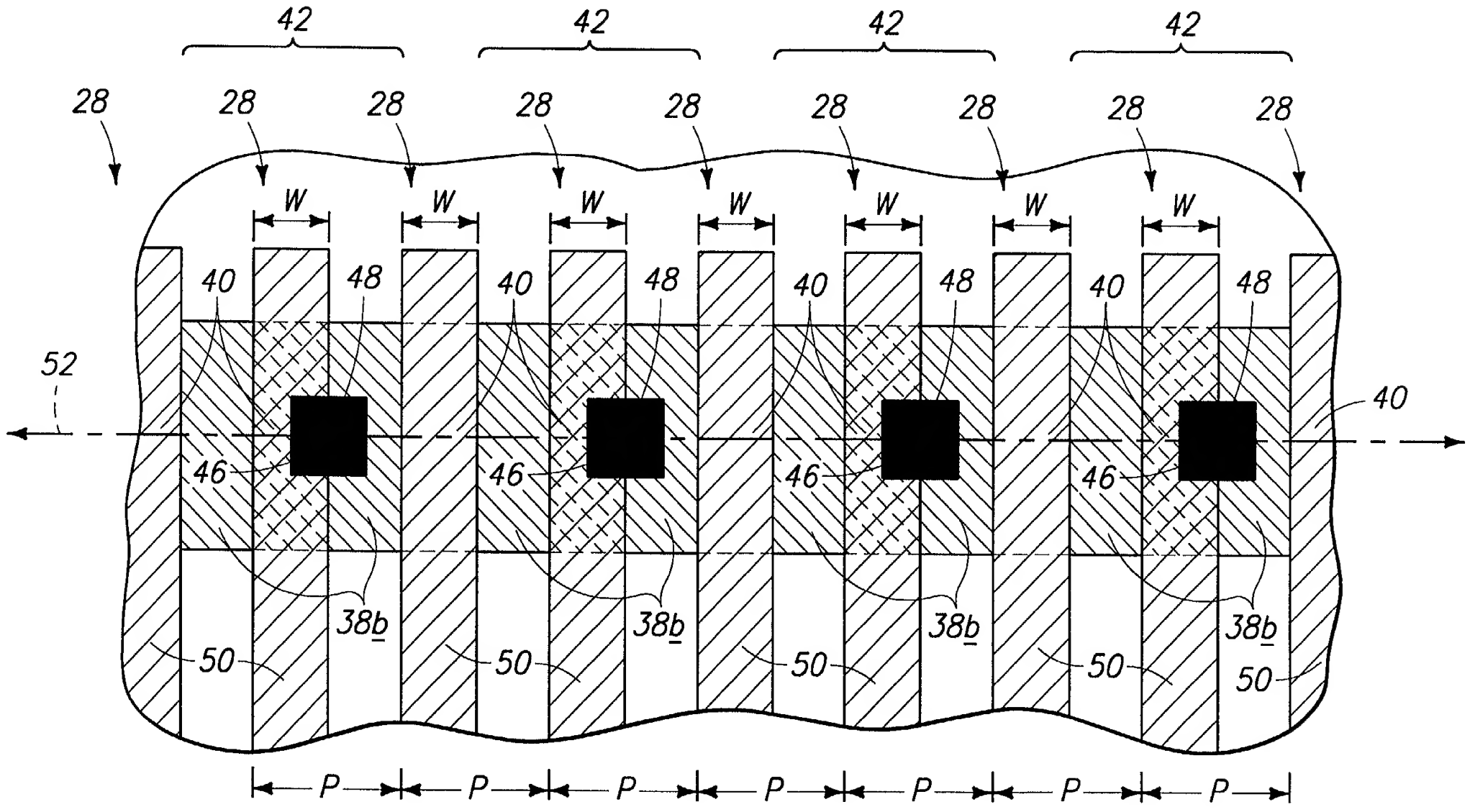
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Fig 4

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming Contacts, Methods of Contacting Lines, Methods of Forming Dynamic Random Access Memory Circuitry, Methods of Operating Integrated Circuitry, Integrated Circuits, Dynamic Random Access Memory Circuitry, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of inventor: **Robert Kerr**

Inventor's Signature: Robert Kerr

Date: 8-26-98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **3089 E. Bonview Drive**
Boise, ID 83712

* * * * * * * * * * *

Full name of inventor: **Brian Shirley**

Inventor's Signature: Brian Shirley

Date: 8/31/98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **2484 Sunshine Drive**
Boise, ID 83712

* * * * * * * * * * *

Full name of inventor: **Luan C. Tran**

Inventor's Signature: _____

Date: _____

Residence: **Meridian, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1125 W. Sandy Ct.**
Meridian, ID 83642

* * * * * * * * * * *

Full name of inventor: **Tyler A. Lowrey**

Inventor's Signature: _____

Date: _____

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **2599 E. Plateau Drive**
Boise, ID 83712

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming Contacts, Methods of Contacting Lines, Methods of Forming Dynamic Random Access Memory Circuitry, Methods of Operating Integrated Circuitry, Integrated Circuits, Dynamic Random Access Memory Circuitry, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

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* * * * * * * * * * *

Full name of inventor: **Robert Kerr**

Inventor's Signature: _____

Date: _____

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **3089 E. Bonview Drive**
Boise, ID 83712

* * * * * * * * * * *

Full name of inventor: **Brian Shirley**

Inventor's Signature: _____

Date: _____

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **2484 Sunshine Drive**
Boise, ID 83712

* * * * * * * * * * *

Full name of inventor: **Luan C. Tran**

Inventor's Signature: _____

Date: _____

Residence: **Meridian, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1125 W. Sandy Ct.**
Meridian, ID 83642

* * * * * * * * * * *

Full name of inventor: **Tyler A. Lowrey**

Inventor's Signature: Tyler A Lowrey

Date: 8/27/98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **2599 E. Plateau Drive**
Boise, ID 83712

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, and Integrated Circuits, Serial No. 09/146,115, filed September 2, 1998.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of inventor: **Luan C. Tran**

Inventor's Signature: Luan C. Tran

Date: 1-18-1999.

Residence: **Meridian, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1125 W. Sandy Ct.**
Meridian, ID 83642

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/146,115
Priority Filing Date ..... September 2, 1998
Inventor ..... Robert Kerr et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2825
Priority Examiner ..... R. Hullinger
Attorney's Docket No. MI22-1343
Title: Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, and Integrated Circuits

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

ASSOCIATE POWER OF ATTORNEY

Please recognize Frederick M. Fliegel, Reg. No. 36,138; D. Brent Kenady, Reg. No. 40,045; James E. Lake, Reg. No. 44,854; and Bernard Berman, Reg. No. 37,279; whose post office address is 601 W. First Avenue, Suite 1300, Spokane, Washington 99201-3828, as associate attorneys or agents in the above-entitled application.

Date: 2/24/00

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Application Number	Priority 09/146,115
Filing Date	Priority 09/02/1998
First Named Inventor	Robert Kerr
Group Art Unit	Priority 2825
Examiner Name	Priority R. Hullinger
Attorney Docket Number	MI22-1343

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Typed or Printed Name	Bernard Berman, Reg. No. 37,279
Signature	Bernard Berman
Date	Feb 24, 2000

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